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EXAMINER	
LUU, CUONG V	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/872,435	BADE ET AL.	
	Examiner	Art Unit	
	Cuong V. Luu	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-88* is/are pending in the application.

4a) Of the above claim(s) *1-36,79-88* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *37-72 and 74-78* is/are rejected.

7)☒ Claim(s) *73* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/25/02, 6/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-88 are pending. Claims 1-36, 79-88 have been withdrawn. Claims 37-78 have been examined. Claim 73 has been objected to. Claims 37-72, 74-78 have been rejected.

Claim Objections

1. Claims 49 and 67 are objected to because of the following informalities:

   1.1. As per claim 49, there is an apparent typographical error in "further comprising the graphical user interface is configured to permit a a user to associate". The error is underlined.

   1.2. As per claim 67, there is an apparent typographical error in "loading a benchmark software application for execution on the virtual evaluation platoform". The error is underlined.

   Appropriate correction is required.

Election/Restrictions

1. Claims 1-21 and 86 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected class 703, subclass 13, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 10/24/2005.

2. Claims 22-36, 79-85, and 87-88 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected class 716, subclass 4, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 10/24/2005.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 52-59, 64 are rejected under 35 U.S.C. 102(b) as being anticipated by Rompaey (E.U. Application 96870126.8).

1. As per claim 52, Rompaey teaches a computer implemented method of embedded system design, the method comprising:

   selecting an instruction set accurate simulator of a target processor core (col. 9, lines 19-27 and 23-25);

   generating a virtual hardware component that is a finite state representation of at least one hardware component; linking read, write, and interrupt signals of the instruction set accurate simulator of the target processor core with corresponding signals of the at least one virtual hardware component to form a virtual embedded system (col. 9, lines 19-22; col. 20, lines 55-58; col. 21, lines 1-14);

   coupling a virtual test bench to at least one signal or variable of the virtual embedded system to simulate a human/machine interface (col. 21, lines 8-16); and

   coupling a software debugger to the virtual embedded system that is configured to load and run on the virtual embedded system at least one binary program executable of a software application compiled for the target processor core (col. 13, lines 39-48. The applicant mentions Coware, and it inherits software debugger feature).

2. As per claim 53, Rompaey teaches selecting the target processor core from a library having a plurality of instruction set accurate simulators for a plurality of processor cores (col. 9, lines 19-27).

3. As per claim 54, Rompaey teaches selecting the virtual hardware component from a library of virtual hardware components (col. 9, lines 23-25).

4. As per claim 55, Rompaey teaches modifying the virtual hardware component (col. 7, lines 43-55).

5. As per claim 56, Rompaey teaches loading benchmark software in an evaluation phase of an embedded system project and running a simulation of the virtual embedded system executing the benchmark software (col. 10, lines 10-13. Benchmark software is a type of application software. Therefore, the examiner interprets Rompaey suggests a benchmark software to be executed on the virtual embedded system).

6. As per claim 57, Rompaey teaches loading binary program executables of development software compiled for the target processor core in a development phase of an embedded systems project and running a simulation of the virtual embedded system executing the development software (col. 10, lines 10-13).

7. As per claim 58, this limitation has already been discussed in claim 52. It is, therefore, rejected for the same reasons.

8. As per claim 59, Rompaey teaches storing the virtual embedded system as a design having at least one executable file in a design repository (col. 17, lines 49-54l col. 32, lines 41-47).

9. As per claim 64, Rompaey teaches a method of designing an embedded system, the method comprising:

defining a system architecture of the embedded system (col. 7, lines 31-35);

designing a virtual prototype of the embedded system having an instruction set accurate simulator of a target processor core coupling read, write, and interrupt signals with a finite machine (FSM) representation of at least one hardware element (col. 20, lines 55-58; col. 21, lines 1-14);

coupling the virtual prototype to a software debugger having a debugging interface and a virtual test bench having a graphical representation of a human/machine interface for interacting with the embedded system (col. 9, lines 19-22; col. 13, lines 39-48. The applicant mentions Coware, and it inherits graphical interface with the embedded system);

developing at least one software application for the processor core (col. 10, lines 10-13);

loading compiled binary program code of the at least one software application for execution of the virtual prototype (col. 10, lines 10-13); and

initiating a simulation of the virtual prototype executing the at least one software application (col. 10, lines 10-13).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

> the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 37-39, 49-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rompaey (E.U. Application 96870126.8) in view of Hellestrand et al (U.S. Patent 6263302 B1).

10. As per claim 37, Rompaey teaches in a computer system having a graphical interface and a design language for forming a finite state machine (FSM) representation of a hardware partition of an embedded system, a method of designing an embedded system, the method comprising:

forming a library of processors including an instruction set accurate simulator for each of the processor cores in the library (col. 9, lines 19-27);

responsive to a first sequence of user commands, selecting at least one of the processor cores from the library as a target processor (col. 9, lines 23-25);

responsive to a second sequence of user commands, forming a virtual embedded system including an instruction set accurate simulator of a target processor core coupling

read, write, and interrupt signals with a finite state machine (FSM) simulation of at least one hardware element (col. 9, lines 19-22; col. 20, lines 55-58; col. 21, lines 1-14);

responsive to a request from the user, loading an executable binary file of a software application compiled for the target processor (col. 13, lines 44-52);

executing a simulation of the virtual embedded system running the software application (col. 21, lines 43-47);

Rompaey does not teach:

responsive to a user request, displaying a graphical representation of the execution of the software on the virtual embedded system that includes a software debugger interface to debug the loaded software and a virtual test-bench having a graphical user interface adapted to interact with the simulation.

Hellestrand et al teach these features (col. 21, lines 39-59).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Rompaey and Hellestrand et al. Hellestrand et al's teachings would have provided interactive control of the simulation and visual examination of outcome.

11. As per claim 38, Rompaey teaches a design language including a plurality of graphical symbols with each graphical symbol having a graphical semantic portion and a textual semantic portion (col. 13, lines 56-58; col. 14, lines 1-4).

12. As per claim 39, Rompaey teaches Verilog design language inheriting these features below (col. 12, lines 9-11):

a start object defining a starting point of the finite state machine at an initialization time, the start object having an output connector activated when the start object is initialized;

a state object for representing a state of the finite state machine;

a decision object having an evaluation field for directing a flow of execution based on a result of an expression in the decision field;

a signal-out object for sending a communication signal; a signal-in object for receiving a communication signal;

a connector object for connecting control flow;

a process object for representing a finite state machine process.

But not these features which Rompaey also teach:

a task object including a field for inputting computer code in the C language for defining a behavior of the task object and a connector port for coupling the task object to other objects (col. 13, lines 56-58; col. 14, lines 1-4);

a symbol object having at least one user-definable pin connector and containing a block or process object: a block object for describing the behavior of one or more processes (col. 13, lines 56-58; col. 14, lines 1-4).

13. As per claim 49, Hellestrand et al teach the graphical user interface comprising:

responsive to a user input, associating a breakpoint of execution with a graphical symbol (col. 21, lines 39-40 and 57-59);

receiving a request to debug software (col. 21, lines 28-37); and

stopping the simulation responsive to a command flow of the FSM representation of the hardware element reaching the graphical symbol of the breakpoint of execution (col. 21, lines 42-44 and 57-59).

14. As per claim 50, Hellestrand et al teach responsive to a user request, single-stepping the simulation to sequential breakpoints of execution in the command flow of the FSM representation of hardware elements (col. 21, lines 53-56).

15. As per claim 51, Hellestrand et al teach responsive to a user request, single-stepping the simulation by a pre-selected number of time units (col. 21, lines 53-56).

Claims 40-41, 43-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rompaey (E.U. Application 96870126.8) in view of Hellestrand et al (U.S. Patent 6263302 B1) as applied to claim 37 above, and further in view of Van Huben et al (U.S. Patent 6094654).

16. As per claim 40, Rompaey teaches storing the virtual embedded system as a design (col. 17, lines 49-54),

but not in a design repository coupled to a server; and

providing access privileges to the design to a selected individual or group.

Van Huben et al teach these features (col. 12, lines 46-54; col. 29, lines 54-59).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Rompaey, Hellestrand et al, and Van Huben et al. Van Huben et al's teachings would have provided reuse capability of the system rather than creating it completely.

17. As per claim 41, Rompaey and Hellestrand et al do not teach responsive to a user command, providing access privileges to the design to a group of vendors.

Van Huben et al teach this feature (col. 29, lines 54-59. The examiner interprets "groups of those who can access it" mentioned in these lines including a group of vendors).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Rompaey, Hellestrand et al, and Van Huben et al. Van Huben et al's teachings would have provided access of the stored embedded system for reuse to a selected group or people.

18. As per claim 43, this limitation has been discussed in claim 41. It is, therefore, rejected for the same reason.

19. As per claim 44, this limitation has been discussed in claim 41. It is, therefore, rejected for the same reason.

20. As per claim 45, Rompaey and Hellestrand et al do not teach a design manager application permitting one or more members of a design team to select edit privileges of at least one version of the design.

Van Huben et al teach this feature (col. 16, lines 19-22; col. 29, lines 54-59).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Rompaey, and Hellestrand et al, and Van Huben et al. Van Huben et al's teachings would have provided selected users capability to access a specific version of a design.

21. As per claim 46, Rompaey and Hellestrand et al do not teach permitting one member of the design team to load and execute a binary program executable of a software application compiled for the target processor core onto the design.

Van Huben et al teach this feature (col. 15, lines 48-55).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Rompaey, and Hellestrand et al, and Van Huben et al. Van Huben et al's teachings would have enabled designers to promote data or run library processes without the need for a data manager to process it.

22. As per claim 47, Rompaey and Hellestrand et al do not teach providing version control and regulating editing access to maintain a consistent version of the design.

Van Huben et al teach these features (col. 16, lines 19-22).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Rompaey, and Hellestrand et al, and Van Huben et al. Van Huben et al's teachings would have provided selected users capability to access a specific version of a design.

23. As per claim 48, these limitations have already been discussed in claim 40. They are, therefore, rejected for the same reasons.

Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rompaey in view of Hellestrand et al as applied to claim 37 above, and further in view of Van Huben et al and Schwab (U.S. Pub. 2004/0250083 A1).

24. As per claim 42, Rompaey, Hellestrand et al, and Van Huben et al do not teach the design is accessible from an on-line bidding board.

Schwab teaches products accessible from an on-line bidding board (p. 10, paragraph 0093).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Rompaey, Hellestrand et al, Van Huben et al, and Schwab. Schwab's teachings would have made the design available to potential buyers online.

Claims 60-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rompaey as applied to claims 52 and 59 above, and further in view of Van Huben et al.

25. As per claim 60, these limitations have already discussed in claim 40. They are, therefore, rejected for the same reasons.

26. As per claim 61, Rompaey does not teach user-group being a geographically distributed embedded system project team.

Huben et al teach this feature (col. 12, lines 61-67; col. 13, lines 10-14).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Rompaey, and Van Huben et al. Van Huben et al's teachings would have enforced provision of a computing environment that can handle distributed computing.

27. As per claim 62, Rompaey does not teach providing a version of the design to a vendor offering a service related to the virtual embedded system.

Huben et al teach this feature (col. 15, lines 48-55).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Rompaey, and Van Huben et al. Van Huben et al's teachings would have allowed vendors to run library processes without the need for a Data Manager to process it.

28. As per claim 63, Rompaey does not teach the design being stored on a server and a vendor being provided access to the design via network connection.

Huben et al teach this feature (col. 15, lines 48-55).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Rompaey, and Van Huben et al. Van Huben et al's teachings would have provided access to vendors at distant locations.

Claim 65-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rompaey in view of Schubert et al (U.S. Pub. 2005/0193280 A1).

29. As per claim 65, Rompaey does not teach developing a hardware implementation using the virtual prototype as a functional specification describing a hardware partition.

Schubert et al teach this feature (p. 2, paragraph 0017).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Rompaey and Schubert et al. Schubert et al's teachings would have enabled running testbench software faster than on virtual prototype.

30. As per claim 66, Rompaey teaches:

evaluating the operation of the embedded system executing the at least one software application (col. 10, lines 10-13); and

responsive to a result of the evaluation, modifying a hardware component of the embedded system (col. 7, lines 43-55).

31. As per claim 67, Rompaey teaches:

selecting at least one embedded system component for evaluation (col. 10, lines 10-13);

forming a virtual evaluation platform including the selected embedded system component (col. 10, lines 10-13);

loading a benchmark software application for execution on the virtual evaluation platform (col. 10, lines 10-13. Benchmark software is a type of application software. Therefore, the examiner interprets Rompaey suggests a benchmark software to be executed on the virtual embedded system); and

evaluating performance of the virtual evaluation platform executing the benchmark software application (col. 10, lines 10-13).

Claims 68-70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rompaey in view of Van Huben et al.

32. As per claim 68, Rompaey teaches a method of providing information to potential suppliers for procuring a good or service associated with an embedded system, the method comprising:

defining a system architecture of the embedded system (col. 7, lines 31-35);

designing a virtual prototype of the embedded system having an instruction set accurate simulator of a target processor core and a virtual hardware element that is a finite state machine (FSM) representation of a hardware element configured to couple memory read/write requests and interrupt signals with the instruction set accurate simulator of the target processor core (col. 20, lines 55-58; col. 21, lines 1-14);

coupling the virtual prototype to a virtual test bench having a graphical representation of a human/machine interface for interacting with the embedded system (col. 9, lines 19-22;

col. 13, lines 39-48. The applicant mentions Coware, and it inherits graphical interface with the embedded system);

Rompaey does not teach:

publishing the virtual prototype as a functional specification from which a vendor may initiate a simulation of the operation of the embedded system.

Van Huben et al teach making a design available to a selected individual or group to dispatch tasks on it (col. 29, lines 54-59; col. 15, lines 48-55).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Rompaey, and Van Huben et al. Van Huben et al's teachings would have provided access of the stored embedded system for reuse to a selected group or people.

33. As per claim 69, storing a design on a computer readable medium and publishing it by sending the computer readable medium to a vendor is very well known. These limitations are, therefore, rejected.

34. As per claim 70, Rompaey does not teach the virtual prototype being published by posting the virtual prototype as a design hosted on a database coupled to the network server.

Van Huben et al teach this feature (col. 12, 46-67; col. 13, lines 1-12).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Rompaey, and Van Huben et al. Van Huben et al's teachings would have provided access of the stored embedded system to users at distant locations.

Claims 71-72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rompaey in view of Van Huben et al as applied to claims 68 and 70 above, and further in view of Schwab.

35. As per claim 71, Rompaey and Van Huben et al do not teach the virtual prototype is published to a bulletin board of the database.

Schwab teaches this feature (p. 10, paragraph 0093).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Rompaey, Van Huben et al, and Schwab. Schwab's teachings would have made the design available to potential buyers online.

36. As per claim 72, Rompaey and Van Huben et al do not teach the bulletin board being a bidding board.

Schwab teaches this feature (p. 10, paragraph 0093).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Rompaey, Van Huben et al, and Schwab. Schwab's teachings would have made the design available to potential buyers to bid online.

Claims 74, 76-78 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Huben et al in view of Rompaey.

37. As per claim 74, Van Huben et al teach a computer-implemented method for a vendor to acquire information for the procurement of a service related to a project, the method comprising:

accessing a database of a design (col. 29, lines 55-59);

instantiating an instance of one of the virtual prototypes (col. 15, lines 48-53); and

evaluating the virtual prototype (col. 15, lines 48-53).

But Van Huben et al do not teach:

The design being a virtual prototype of embedded system, each of the virtual prototypes having a processor simulator, a finite state machine representation of hardware peripherals, and a virtual test bench emulating a human/machine interface for interacting with a simulation of the operation of the virtual prototype.

Rompaey teaches this feature (col. 20, lines 55-58; col. 21, lines 1-14; col. 9, lines 19-22; col. 13, lines 39-48).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Van Huben et al and Rompaey. Rompaey's teachings would have made a virtual prototype of embedded system accessible for evaluation.

38. As per claim 76, Van Huben et al teach the design configured to show a parts list (col. 20, lines 5-8) but do not teach the design being the virtual prototype.

Rompaey teaches this feature (col. 20, lines 55-58; col. 21, lines 1-14; col. 9, lines 19-22; col. 13, lines 39-48).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Van Huben et al and Rompaey. Rompaey's teachings would have made the part list available to users to track their synchronization.

39. As per claim 77, Van Huben et al teach the design configured to show a component net list (col. 151, lines 6-9) but do not teach the design being the virtual prototype.

Rompaey teaches this feature (col. 20, lines 55-58; col. 21, lines 1-14; col. 9, lines 19-22; col. 13, lines 39-48).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Van Huben et al and Rompaey. Rompaey's teachings would have allowed building models from released data.

40. As per claim 78, Van Huben et al teach the database of designs being hosted on a network server accessible by a client computer (col. 12, 46-67; col. 13, lines 1-12).

Claims 75 is rejected under 35 U.S.C. 103(a) as being unpatentable over Van Huben et al in view of Rompaey as applied to claim 74 above, and further in view of Schwab.

41. As per claim 75, Van Huben et al and Rompaey do not teach submitting a quote for a good or service related to the embedded system simulated by the virtual prototype.

Schwab teaches submitting a quote for a good or service related to a product (p. 4, paragraph 0038).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Rompaey, Van Huben et al, and Schwab. Schwab's teachings would have allowed bid on a good or service related to the embedded system simulated by the virtual prototype.

Allowable Subject Matter

Claim 73 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

42. As per claim 73, it is objected to as being dependent upon a rejected base claim 70, but would be allowable if rewritten in independent form including all of the limitations of the base claim including the following limitation which makes it allowable:

wherein the virtual prototype is published to a database having a matching engine.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cuong V. Luu whose telephone number is 571-272-8572. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah, can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. An inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CVL

Thai Phan
Patent Examiner
Au: 2128
12/21/05